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EFFICIENT GLOBAL 'RAPID' OPTIMIZATION OF ANALOG CIRCUITS: APPLICATION TO THE DESIGN OF A CMOS OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

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ABSTRACT
Main goals of analog circuit sizing optimization are to maximize circuits' performances within a reasonable computing time. This allows designers reducing the so-called time to market. Recently, it has been proven that the efficient global optimization (EGO) technique allows constructing accurate models of circuits (not only) performances. Evaluation of such analytical models is very fast when compared to the well-known inloop techniques. In this work we focus on adopting such EGO technique for the optimal design of 'complex' analog CMOS circuits. The case of an operational transconductance amplifier sizing problems is considered. Comparison with two metaheuristic-based in loop sizing techniques (PSO and BSA) is provided to show efficiency and rapidity of the proposed EGO-based approach.

KEYWORDS: EGO algorithm, Expected improvement, Meta-modeling, Kriging, metaheuristics, DE, PSO, BSA,CMOS, OTA.

1. INTRODUCTION
Analog circuit design is a complex and delicate task[1-3]. Therefore, performing optimization is indispensable to assure high performances. Two optimization approaches are proposed in the literature [4,5]: the equation-based approach and the in-loop one. The latter is more accurate than the former technique. Nevertheless, its main drawback is its slowness. Contrariwise, the equation-based approach is characterized by its rapidity. Surrogate modeling bid an excellent solution to gather benefits of both aforementioned techniques [6-8].

Nowadays, surrogate models are widely used to replace expensive simulations [9,10]. These modeling techniques are able to approximate very complex non-linear functions by a simple and an accurate model. The specialized literature offers a very large spectrum of surrogate model techniques [6-12]. Among them, we are interested in the Kriging model. As compared to the other modeling techniques, the Kriging approach offers several advantages, such as the simplicity of its implementation, the accuracy of constructing models, and the fact that it is able to provide an estimation of the model's error. Furthermore, these models can be easily integrated within optimization routines.

Efficient global optimization (EGO) algorithm is one of the most widely used surrogate-based optimization algorithms [13]. EGO starts by building a kriging model based on a few initial samples. Then, according to the expected improvement (EI) criterion[13]precision of the model under construction is improved by adding supplementary samples. The EI criterion is considered for this purpose [14].

In this work, we focus on adapting EI- based EGO for the enhancement of analog circuit performances. It is to be stated that a first draft of this idea has already been proposed in [15] where the application of EI has been validated on an OTA [16]. In this work, we consider the maximization of three main performances of an OTA, namely, its voltage gain, its common mode rejection ratio (CMRR) and its positive power-supply rejection ratio (PSRR).Effectiveness, regarding accuracy and rapidity, of the proposed approach is stressed via a comparison with two metaheuristic-based in loop optimization. Two well-known rapid met heuristics are considered:

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particle swarm optimization (PSO) and backtracking search optimization (BSA).Furthermore, the efficiency of our approach is showcased via solving a complex analog CMOS circuit with a relatively large number of variables.

The rest of this paper is organized as follows. In Section II and III, we give a brief description of the EGO algorithm and of both considered metaheuristic-based in loop optimization approaches. In Section IV, we present the application of three algorithms for the optimal design of the considered analog circuit. Finally, the last section highlights some concluding remarks.

2. OVERVIEW OF THE EFFICIENT GLOBAL OPTIMIZATION ALGORITHM

EGO has been proposed by Donald R. Jones in 1998 [13]. The algorithm adapts a Kriging model to an initial sampling design by evaluating an objective function. At each iteration, the point with the maximum expected improvement (EI) value is selected and evaluated to update the Kriging model. Each time, a set of samples is added to the initial design in order to decrease the prediction error. The optimization process of the EI function is based on the Differential Evolution (DE) algorithm [17].

The pseudocode of the EGO algorithm can be presented as follows, see Algorithm 1:

Algorithm 1 *The EGO pseudocode*

Create an initial design: $\mathbf{X} = [\mathbf{x}_1; : : : ; \mathbf{x}_n]$
Evaluate function at $\mathbf{X}$ *and set* $\mathbf{Y} = f(\mathbf{X})$.
The best result ($\mathbf{x}min$, $ymin$)
While *the stop criterion is not met* ***do***
Fit a kriging model on the data points ($\mathbf{X}$; $\mathbf{Y}$).
$\mathbf{x}_{n+1} \leftarrow$ *maximize EI (max E I* ($\mathbf{x}$)) *and add* $\mathbf{x}_{n+1}$ *to* $\mathbf{X}$.
$y_{n+1} \leftarrow f(\mathbf{x}_{n+1})$ *and add yn+1 to* $\mathbf{Y}$.
$ymin \leftarrow min(\mathbf{Y})$ *(Compute the minimum ymin)*
$\mathbf{x}min \leftarrow \mathbf{x} \in \mathbf{X}$: $y(\mathbf{x}) = ymin$
Re-estimate the parameters and update the Kriging model.
end while

The core of the EGO algorithm is based on the use of three routines: The first, i.e. uses the Kriging technique for constructing the model. The second makes appeal to the Expected improvement criterion to improve accuracy of the model under construction. The third routine is a metaheuriticthat maximizes EI. The differential evolution (DE) metaheuristic is used. Respective details are given in the following sub-sections.

1. *Krigingmetamodeling technique*

The Kriging is one of the most popular surrogate modeling technique used in approximating computationally expensive functions and generating accurate models of complex and non-linear systems [11]. Kriging approach was proposed by Daniel G.Krige to predict the spatial patterns for gold mines[18].Later, the Kriging model has been used to improve the approximation of computer experiments[19].
The approximation function of the Kriging model can be formulated as follows:

$$y(x) = \mu + \varepsilon(x) \tag{1}$$

where the mean of the Gaussian process is $\boldsymbol{\mu}$, the error term $\boldsymbol{\varepsilon(x)}$is normally distributed with mean zero and variance $\boldsymbol{\sigma^2}$. The error term between two points $\boldsymbol{x^{(i)}}$and $\boldsymbol{x^{(j)}}$ are not dependent, their correlation is defined by parameters $\boldsymbol{P_k}$and $\boldsymbol{\theta_k}$:

$$corr\left[\varepsilon\left(x^{(i)}\right),\varepsilon\left(x^{(j)}\right)\right] = \exp\left(-\sum_{k=1}^{d}\theta_k \left|x_k^{(i)} - x_k^{(j)}\right|^{P_k}\right) \tag{2}$$

where ***d*** is the dimension of the design values, this distance is measured by parameters $P_k$and θ_k.$d$is small, hencea large correlation, and large distance means a small correlation. Then, the best linear predictor and the mean squared error of the predictor can be derived in form:

$$\hat{y}(x) = \hat{\mu} + r^T R^{-1}(y - 1\hat{\mu}) \tag{3}$$

and

$$\hat{s}^2(x) = \hat{\sigma}^2 \left[1 - r^T.R^{-1}.r + \frac{\left(1 - 1^T.R^{-1}.r\right)^2}{1^T.R^{-1}.1} \right] \tag{4}$$

where$\hat{\mu}$and $\hat{\sigma}^2$are estimations of $\mu$and σ^2derived by maximizing the likelihood of the observed samples.

with $R_{ij} = corr\left[\varepsilon\left(x^{(i)}\right), \varepsilon\left(x^{(j)}\right)\right]$; $r_i = corr\left[\varepsilon(x), \varepsilon(x^{(i)})\right]$ and $y = \left(y^{(1)}, y^{(2)}, \cdots, y^{(n)}\right)$is the vector of the n observed function value.

2. *The expected improvement criterion (EI)*

As it is aforementioned, the Kriging model can provide both the estimation and the uncertainty of that prediction. Availability of the uncertainty makes the Kriging model very suitable to provide the efficient infill sampling criteria also called the expected improvement (EI).

EI expression can be formulated as given by equation (5).

$$EI(x) = \left(f_{\min} - \hat{y}(x)\right).\Phi\left(\frac{f_{\min} - \hat{y}(x)}{s(x)}\right) + s(x).\phi\left(\frac{f_{\min} - \hat{y}(x)}{s(x)}\right) \tag{5}$$

where f_{min} is the current best observed value, $\hat{y}(x)$is the predictor. ϕ is the standard normal density and Φ is the distribution function. ***s(x)*** is the square root of the Kriging prediction variance. More details can be found in [13]. Actually, EI balances between seeking promising areas of the design space and the uncertainty in the model. According to the equation (5), the first term is large when surrogate prediction decreases, which will lead the search to the local exploitation around the best-observed point. The second term of the expected improvement criterion increases when the variance ***s(x)*** is large. This condition will insure a global exploration of the design space.

3. *Differential evolution (DE)*

The DE algorithm was used within the EGO algorithm in the interest to optimize the EI function performance. Differential evolution is a stochastic metaheuristic algorithm. It is inspired from genetic algorithms(GA) and the evolutionary strategies (ES) combined with geometric search techniques. GA allows changing the structure of the individuals using the mutation and crossover, whereas ES realizes the self-adaptation by a geometric manipulation of the individuals [17].

4. *METAHEURISTICS BASED IN-LOOP OPTIMIZATION*

Inloop based optimization offers a wide spectrum of advantages when compared to the equation-based approach [4,5]. It has already been widely used in analog circuit design. In brief, this technique uses a SPICE-like simulator for evaluating the circuit performances and its intrinsic/extrinsic constraints within an optimization routine, thus avoiding the use of inaccurate equivalent (linearized) circuits' models. In that process, a metaheuristic is used to guide simulator to the optimal values.

Metaheuristics are easy to be implemented and adapted to different problems and they are relatively more rapid and less complex when compared to the conventional mathematical optimization techniques [20], particularly, population based ones.

In our work a particular interest is accorded to two famous techniques: The Backtracking Search Optimization (BSA) [21-22] and the Particle Swarm Optimization (PSO) [23]. This argued by the fact that both techniques are very rapid and well suited to be implemented within an inloop-based sizing technique.

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The flowchart of the in loop optimization approach is presented in Figure 1.

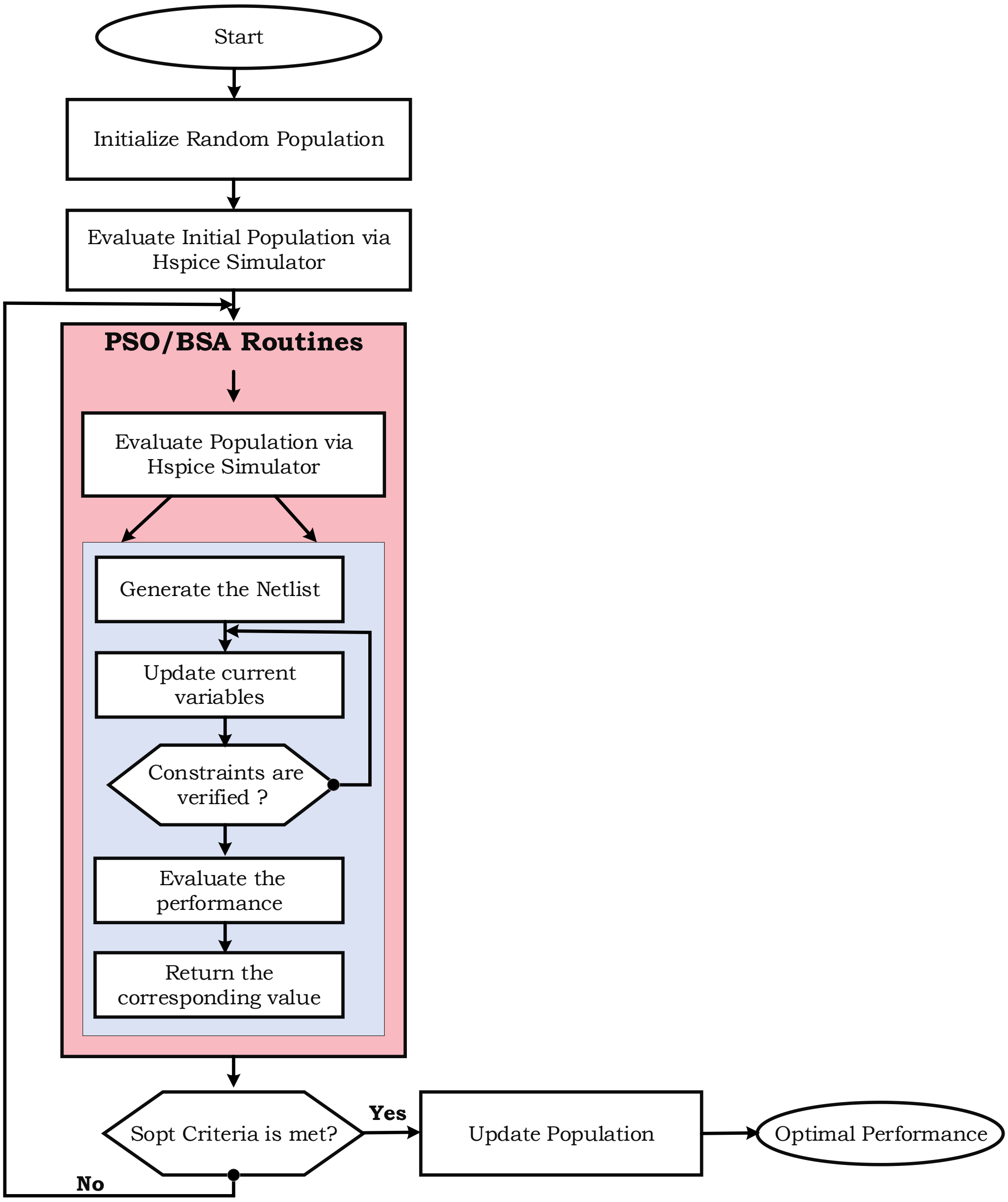

Figure 1. Flowchart of the Metaheuristic algorithms based in-loop optimization

1. *Backtracking Search Optimization*

The Backtracking Search Algorithm (BSA) is a population-based iterative evolutionary algorithm (EA).Main feature of BSA consists of the single control parameter. It has better convergence behavior[21] when compared to other swarm intelligence -based optimization techniques. The flow of the BSA algorithm can be explained by dividing its functions into five processes as is done in other EAs: initialization, selection-I, mutation, crossover, and selection-II. More details are presented in the following references[21-22].

2. *Particle Swarm Optimization (PSO)*

The Particle Swarm Optimization (PSO) approach has been proposed in 1995 by Kennedy and Eberhart [24]. This approach is inspired from the metaphor of social interaction observed among insects and animals. The kind

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of social interaction modeled within a PSO is used to guide a population of individuals (particles) moving toward the most promising area of the search space. We refer the reader to [23] for further details regarding PSO.

3. APPLICATION OF EGO TO THE OPTIMAL DESIGN OF AN OTA

In this section, we present the application of EGO to optimize performances of a CMOS OTA [16]. The considered performances are: the voltage gain, the transition frequency, the common mode rejection ratio (CMRR) and the positive power-supply rejection ratio (PSRR).

The OTA under consideration is shown in Figure 2. This circuit encompasses a differential stage, formed by NMOS transistors (M_9-M_{10}). Transistors M_{11} and M_{12} supply the DC bias voltage to the transistors (M_1-M_2) and (M_7, M_8), respectively. Transistors (M_{13}, M_{15}) and (M_{14}, M_{16}) ensure the differential pair current bias [16].

The model's variables are the channels widths W_N, W_P and the channel lengths L_N, L_P of the NMOS and PMOS transistors, respectively. All transistors are constrained to operate in the saturation mode; AMS 0.35µm technology has been used. (Vdd/Vss=±1.8V, I_{bias1}=60µA, I_{bias2}=90µA).

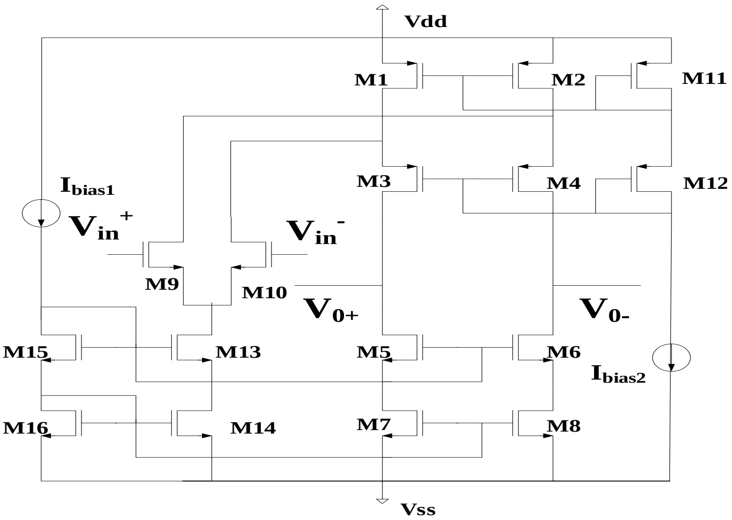

Figure 2. A CMOS operational transconductance amplifier

In the following we give results and respective comparisons upon the application of the proposed EGO-based technique to an eight-variable-OTA-circuit, as well as obtained results via both metaheuristic-based inloop approaches. Two study cases are considered: a population size of 50 individuals and a 50-iteration stopping criterion, and a 100-population and 100 iterations as a stopping criterion. Channel widths and channel lengths of the circuit's MOS transistors are the circuits' variables. Corresponding variation range for W_i ($i\in\{1, 2,3,4\}$) is [20µm,90µm] and for L_i ($i\in\{1, 2,3,4\}$) is [0.35µm,1.2µm]. Table I depicts the considered variables.

TABLE I. TRANSISTORS' VARIABLES OF THE OTA

Transistors	*Variables*
M1, M2, M11	W1,L7
M3, M4	W2,L8
M12	1.5 W2
M5, M6, M7, M8, M13, M14, M15, M16	W3,L5
M10, M9	W4,L6

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Tables II, IV, and VI summarize the optimization results and give the computing time of the considered performances, respectively. Tables III, V, and VII present the corresponding parameters' optimal values, respectively. Corresponding simulation results are presented in Figures 3-5.

TABLE II. COMPARATIVE RESULTS OF THE VOLTAGE GAIN

	Optimization result (dB)	Simulation result H-SPICE (dB)	Relative Error (%)	Execution time
50 samples and 50 iterations				
EGO	87.847	87.801	***0.05***	***58 sec.***
PSO-based in-loop	89.677			***33 min. 25 sec.***
BSA-based in-loop	87.960			***33 min. 51 sec.***
100 samples and 100 iterations				
EGO	88.971	88.981	***0.01***	***3 min. 10 sec.***
PSO-based in-loop	89.677			***2 hr. 10 min. 30 sec.***
BSA-based in-loop	89.587			***2 hr. 33 sec.***

TABLE III. OPTIMAL VARIABLE VALUES OF THE VOLTAGE GAIN

Parameters Values (µm)	*PSO-based in-loop*	*BSA-based in-loop*	*EGO*
50 samples and 50 iterations			
W_1	51.69	80.66	22.02
W_2	90.00	20.00	76.94
W_3	90.00	62.66	89.79
W_4	90.00	60.83	81.45
L_1	1.20	1.06	0.99
L_2	1.01	1.20	1.16
L_3	1.20	0.86	1.20
L_4	1.20	0.35	1.09
100 samples and 100 iterations			
W_1	50.14	90.00	43.15
W_2	90.00	33.74	89.00
W_3	90.00	90.00	77.96
W_4	90.00	20.00	84.65
L_1	1.20	0. 84	1.19
L_2	1.02	1.20	0.95
L_3	1.20	1.20	1.19
L_4	1.20	0.35	1.11

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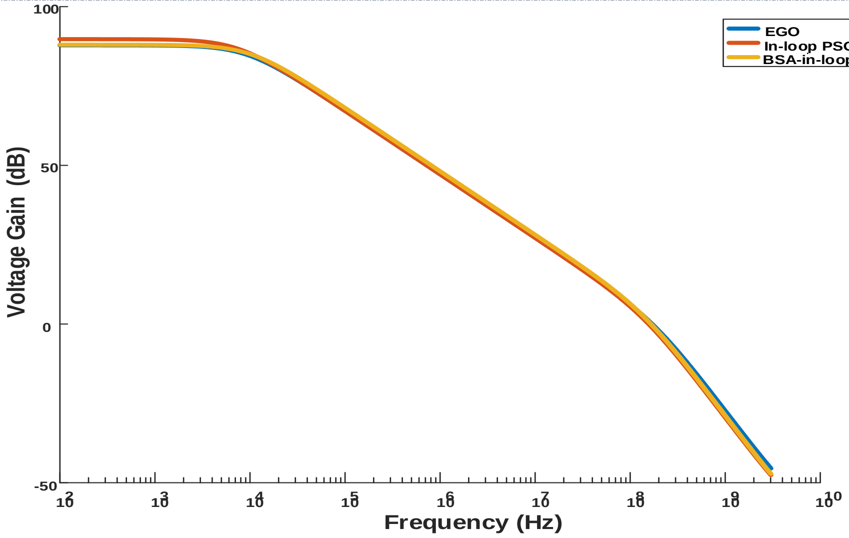

Figure 3. Hspice simulation of the OTA: Voltage Gain

TABLE IV. COMPARATIVE RESULTS OF THE COMMON MODE REJECTION RATIO

	Optimization result (dB)	Simulation result H-SPICE (dB)	Relative Error (%)	Execution time
		50 samples and 50 iterations		
EGO	98.729	99.056	***0.3***	***1 min. 6 sec.***
PSO-based in-loop	102.180			***1 hr. 46 min. 24 sec.***
BSA-based in-loop	99.287			***1 hr. 41 min.***
		100 samples and 100 iterations		
EGO	100.157	99.627	***0.5***	***3 min.***
PSO-based in-loop	102.190			***6 hr. 47 min. 22 sec.***
BSA-based in-loop	108.400			***6 hr. 37 min. 44 sec.***

TABLE V. OPTIMAL VARIABLE VALUES OF THE COMMON MODE REJECTION RATIO

Parameters Values (μm)	***PSO-based in-loop*** (μm)	***BSA-based in-loop*** (μm)	***EGO*** (μm)
	50 samples and 50 iterations		
W_1	20.00	65.39	88.34
W_2	20.00	20.00	22.30
W_3	89.87	90.00	86.11
W_4	90.00	90.00	85.49
L_1	1.20	1.04	1.10
L_2	0.96	1.01	1.03
L_3	0.35	0.35	0.35
L_4	0.35	0.51	1.05
	100 samples and 100 iterations		
W_1	20.00	20.00	75.06
W_2	20.00	90.00	20.00
W_3	90.00	42.57	87.72

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W4	90.00	43.74	90.00
L1	1.20	0.67	1.14
L2	0.97	0.38	0.94
L3	0.35	0.42	0.35
L4	0.35	0.35	0.91

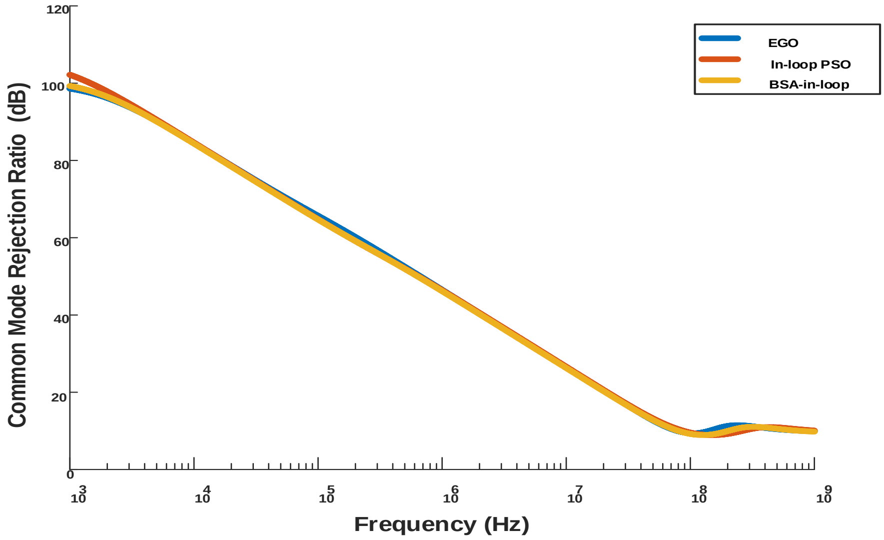

Figure 4. Hspice simulation of the OTA : Common mode rejection ratio

TABLE VI. COMPARATIVE RESULTS OF THE POWER-SUPPLY REJECTION RATIO

	Optimization result (dB)	Simulation result H-SPICE (dB)	Relative Error (%)	Execution time
		50 samples and 50 iterations		
EGO	80.831	80.542	***0.3***	***1 min. 3 sec.***
PSO-based in-loop	81.377			***1 hr. 47 min. 2 sec.***
BSA-based in-loop	80.376			***1 hr. 46 min. 20 sec.***
		100 samples and 100 iterations		
EGO	81.412	80.744	***0.8***	***3 min. 18 sec.***
PSO-based in-loop	81.377			***7 hr.***
BSA-based in-loop	81.239			***6 hr. 46 min. 33 sec.***

TABLE VI. OPTIMAL VARIABLE VALUES OF THE POWER-SUPPLY REJECTION RATIO

Parameters Values (µm)	***PSO-based in-loop*** (µm)	***BSA-based in-loop*** (µm)	***EGO*** (µm)
	50 samples and 50 iterations		
W1	90.00	48.65	35.88
W2	90.00	90.00	90.00
W3	90.00	76.07	90.00
W4	89.99	90.00	90.00
L1	1.20	1.20	1.03
L2	0.99	0.85	0.88

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***L*₃**	1.20	1.20	1.16
***L*₄**	1.20	1.07	1.20
100 samples and 100 iterations			
***W*₁**	89.68	54.33	60.71
***W*₂**	90.00	20.00	90.00
***W*₃**	90.00	90.00	70.04
***W*₄**	89.99	90.00	90.00
***L*₁**	1.20	1.20	1.07
***L*₂**	0.99	0.35	0.87
***L*₃**	1.20	0.35	1.20
***L*₄**	1.20	1.03	1.20

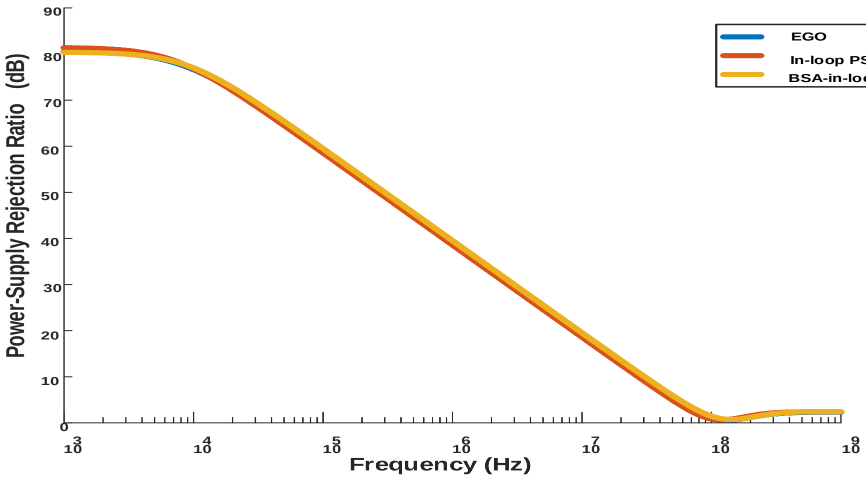

Figure 5. Hspice simulation of the OTA: Power-Supply Rejection Ratio

4. CONCLUSION

In this paper, we introduced the efficient global optimization (EGO) algorithm and we proposed an EGO-based approach for the optimal design of analog circuits. Efficiency of the proposed sizing technique is showcased via the sizing of an CMOS OTA. Considered performances are its voltage gain, its common mode rejection ratio and its positive power-supply rejection ratio. For the sake of comparison with nowadays used 'high performance' sizing techniques, obtained results in terms of accuracy and execution time have compared with those obtained using a PSO-based in loop and an BSA-based inloop sizing techniques. Obtained results show that our approach offers similar accuracy while considerably reducing computing time. This proves that our approach is more interesting and can, without a doubt, be integrated within an CAD tool.

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